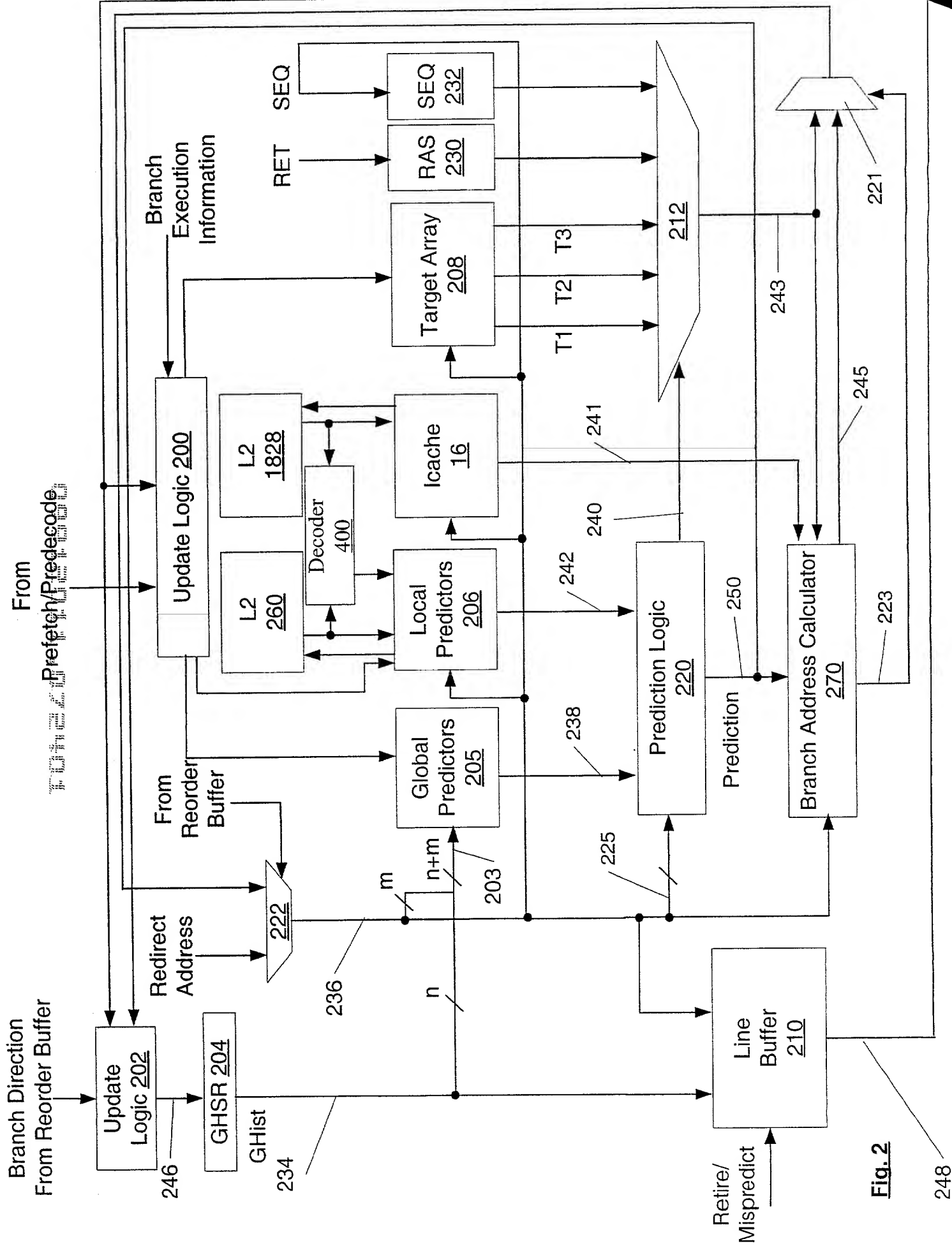


Fig. 1



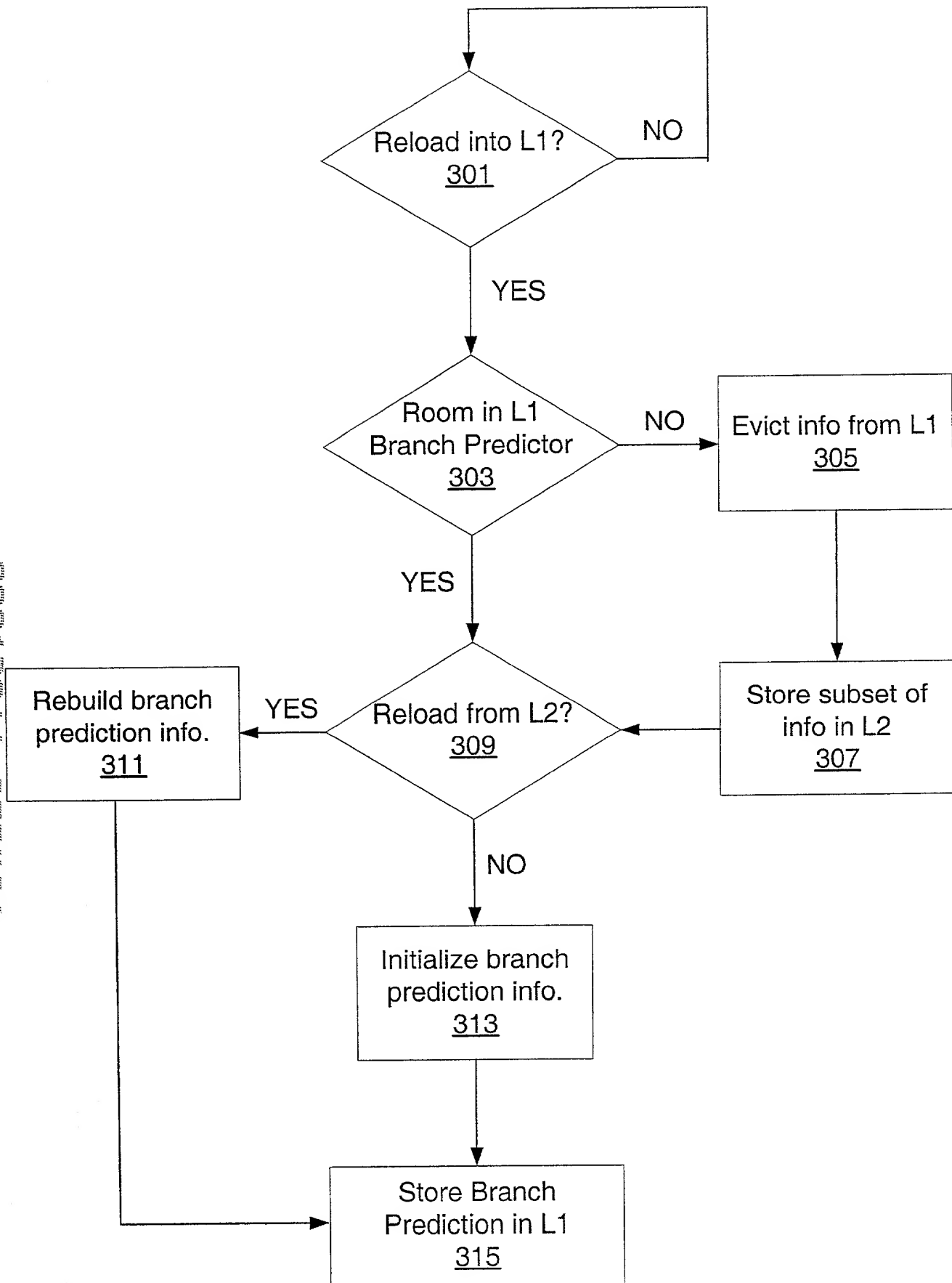


Fig. 3

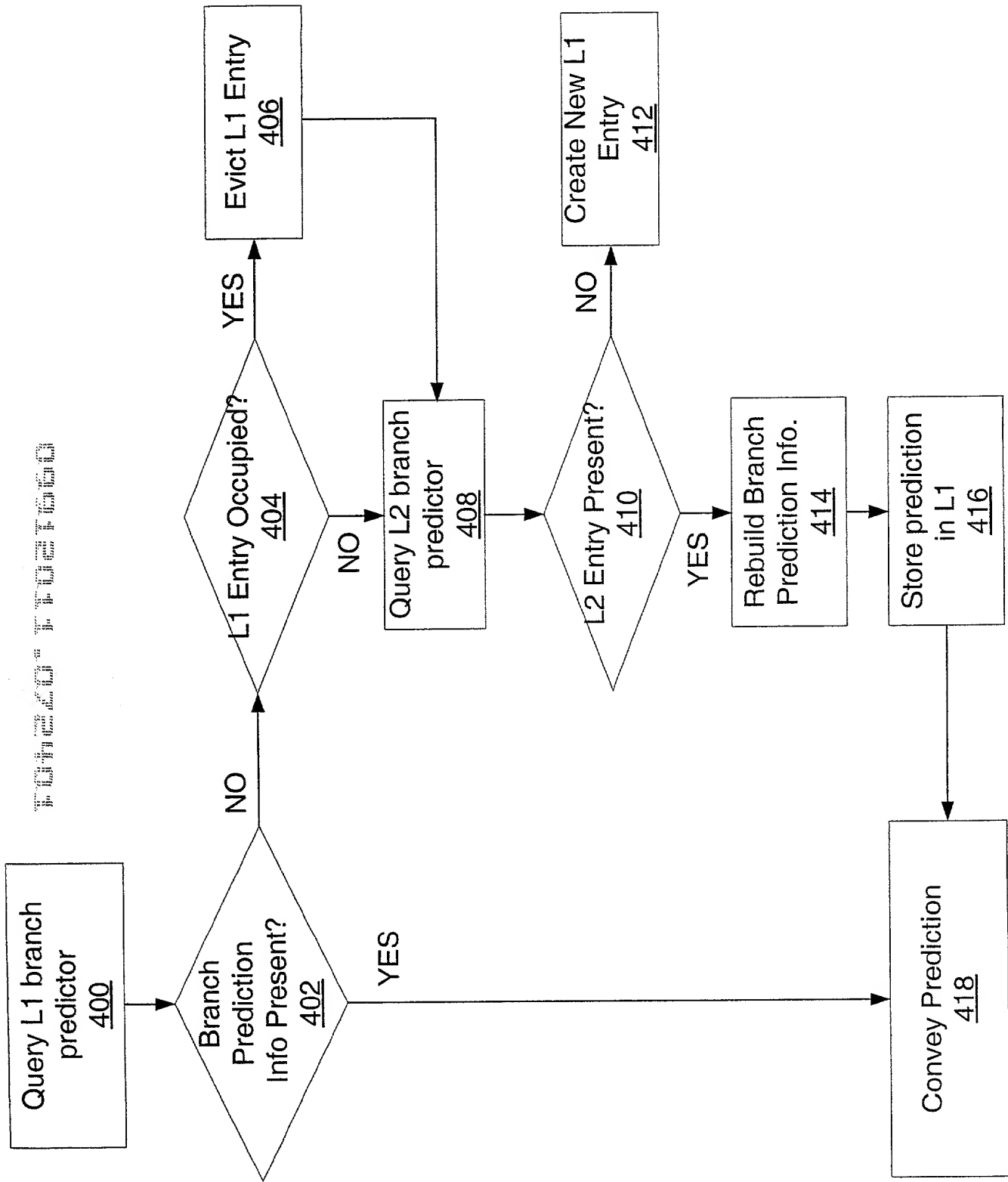
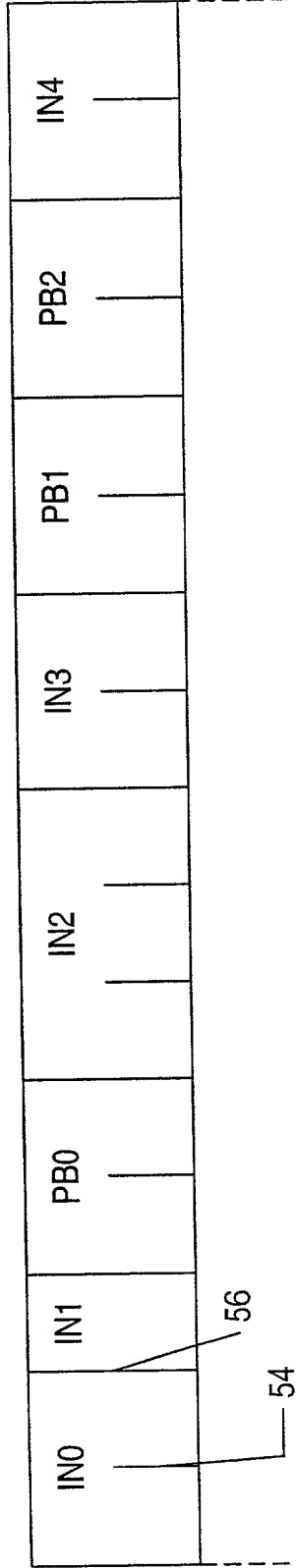


Fig. 4

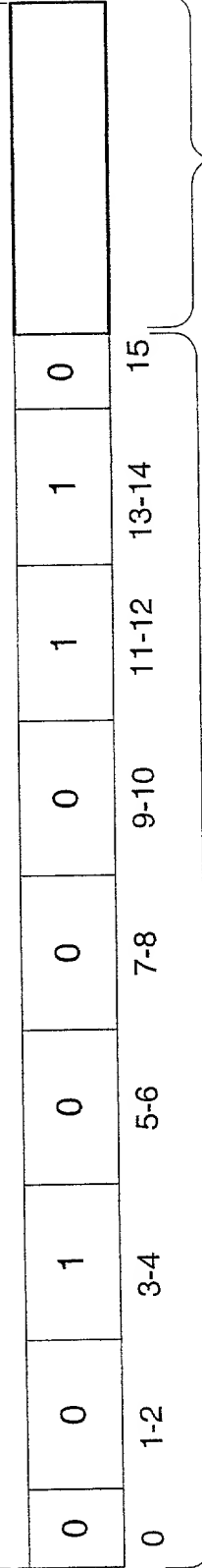
Instruction
Byte #

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15



Marker Bit
#

0 1 2 3 4 5 6 7 8



Branch ending
in bytes

15

450

52

Fig. 5

Offset	<=0	<=1	<=3	<=5	<=7	<=9	<=11	<=13	<=15
	0	1	2	3	4	5	6	7	8
Marker Bit #									

Fig. 6

50

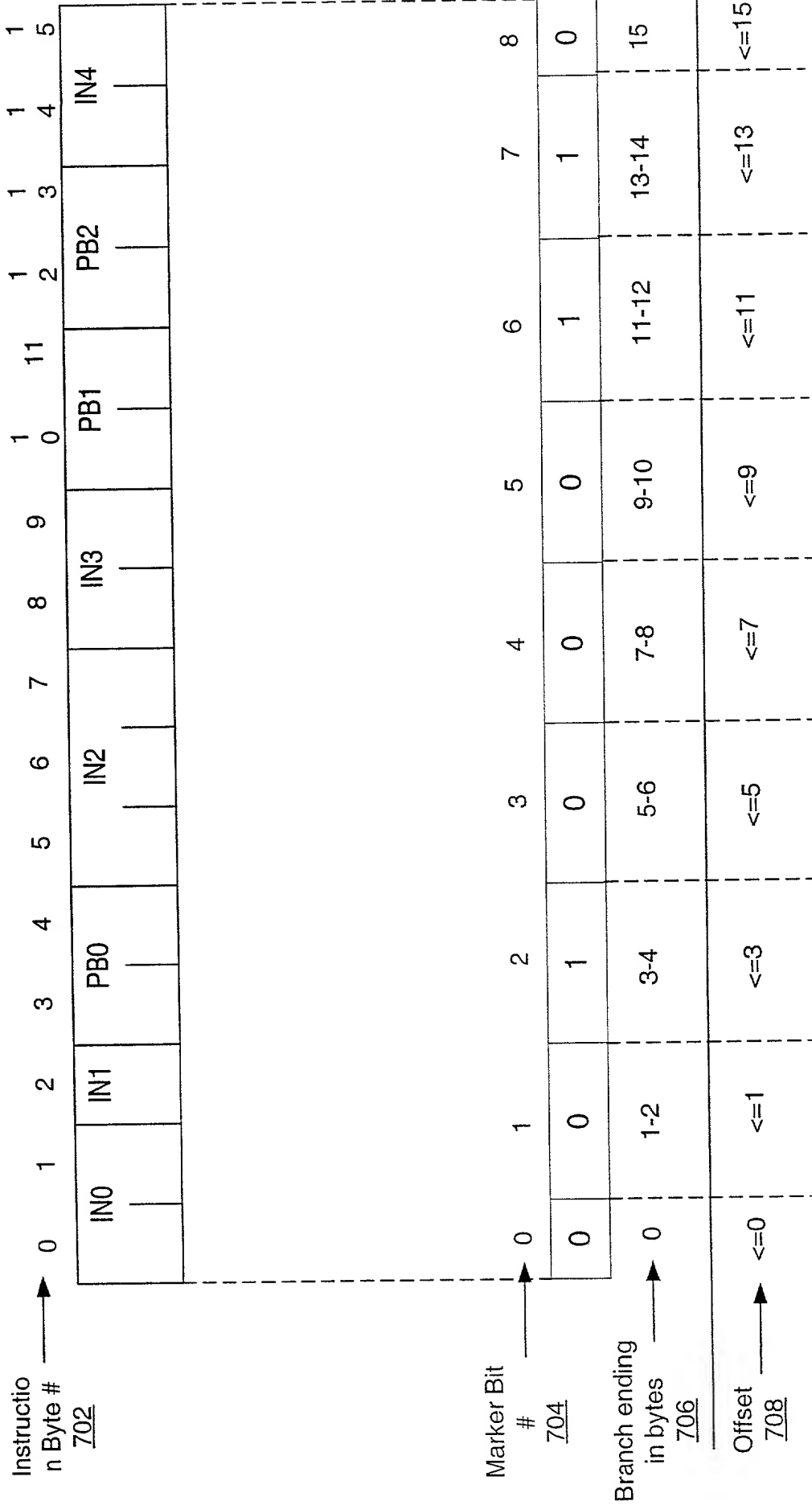


Fig. 7

52

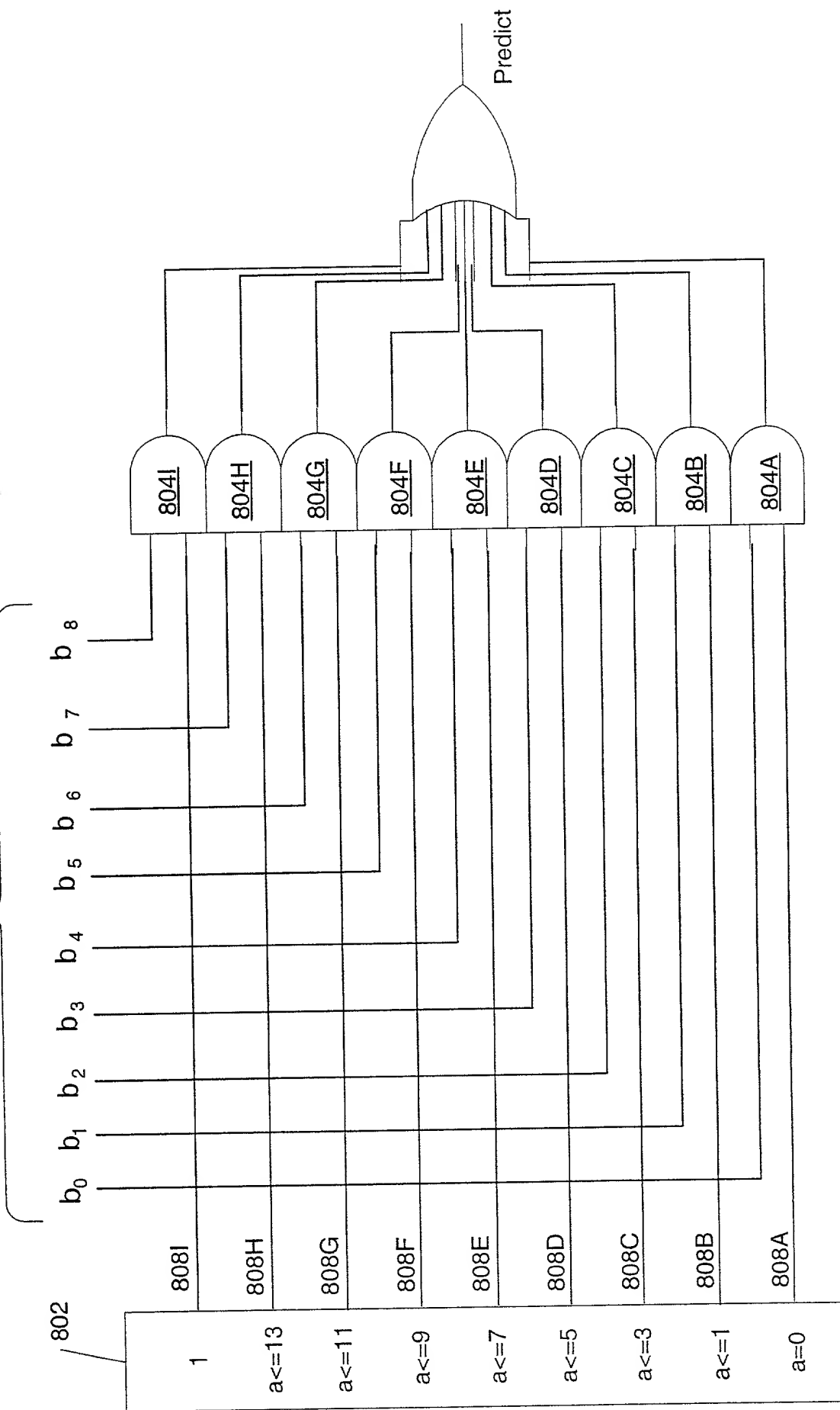


Fig. 8

900

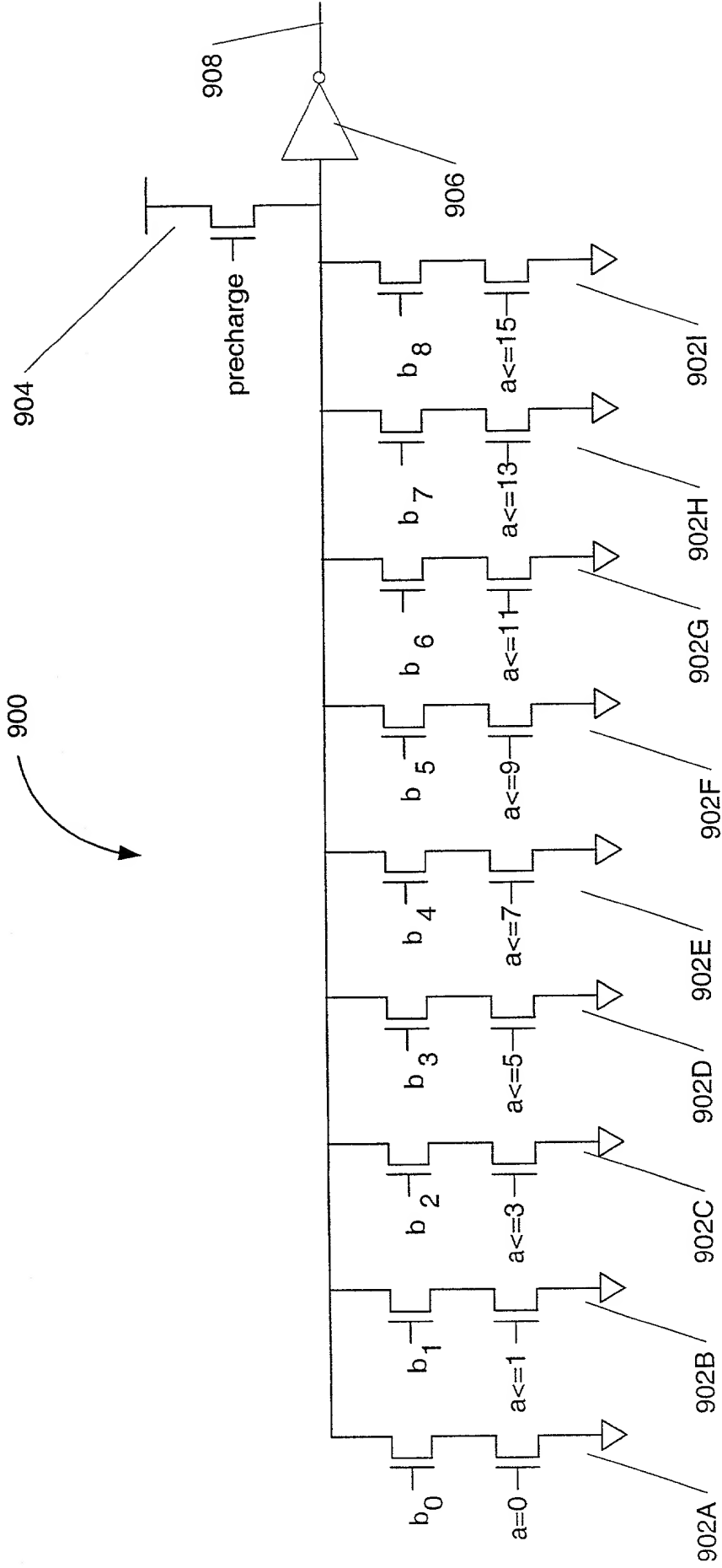


Fig. 9

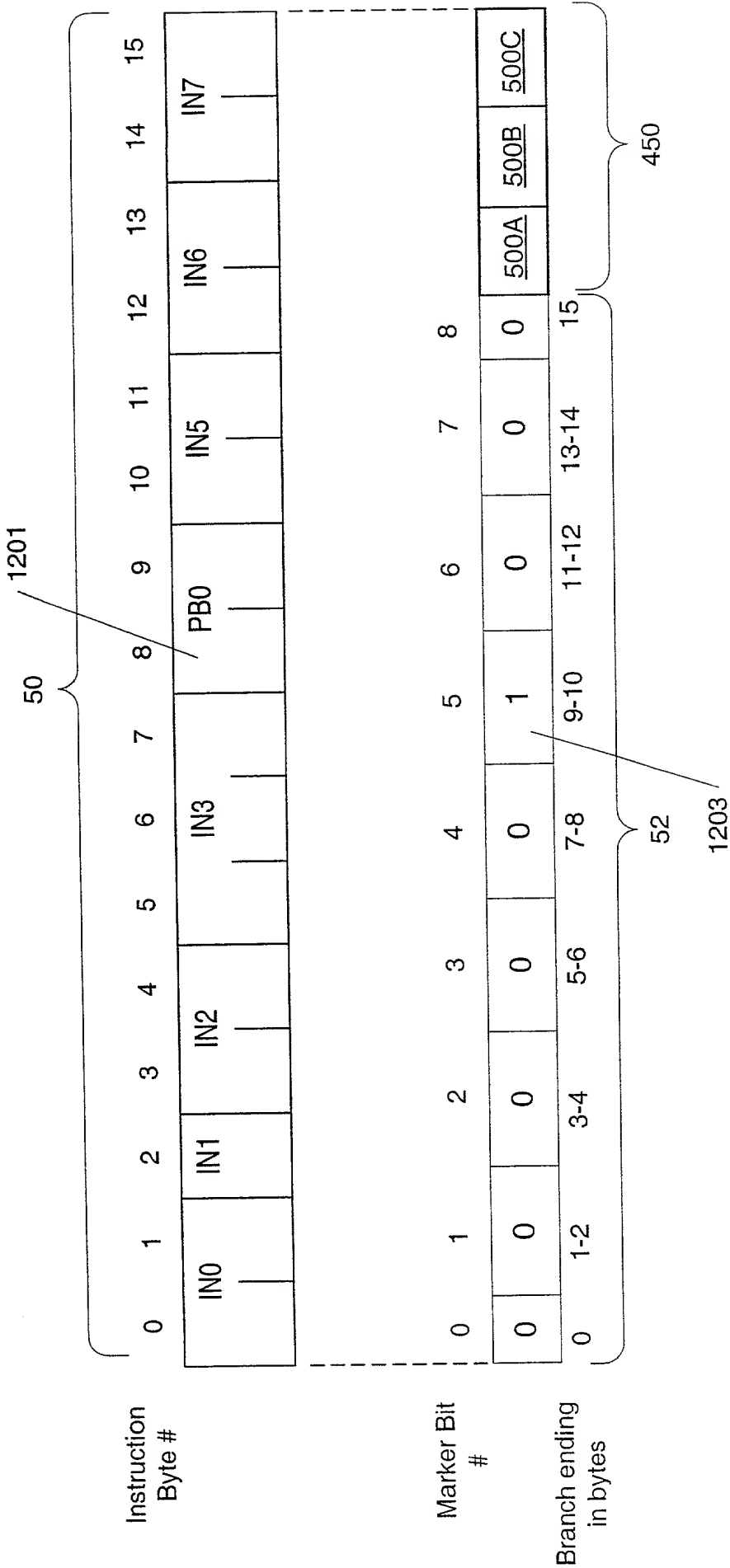


Fig. 11

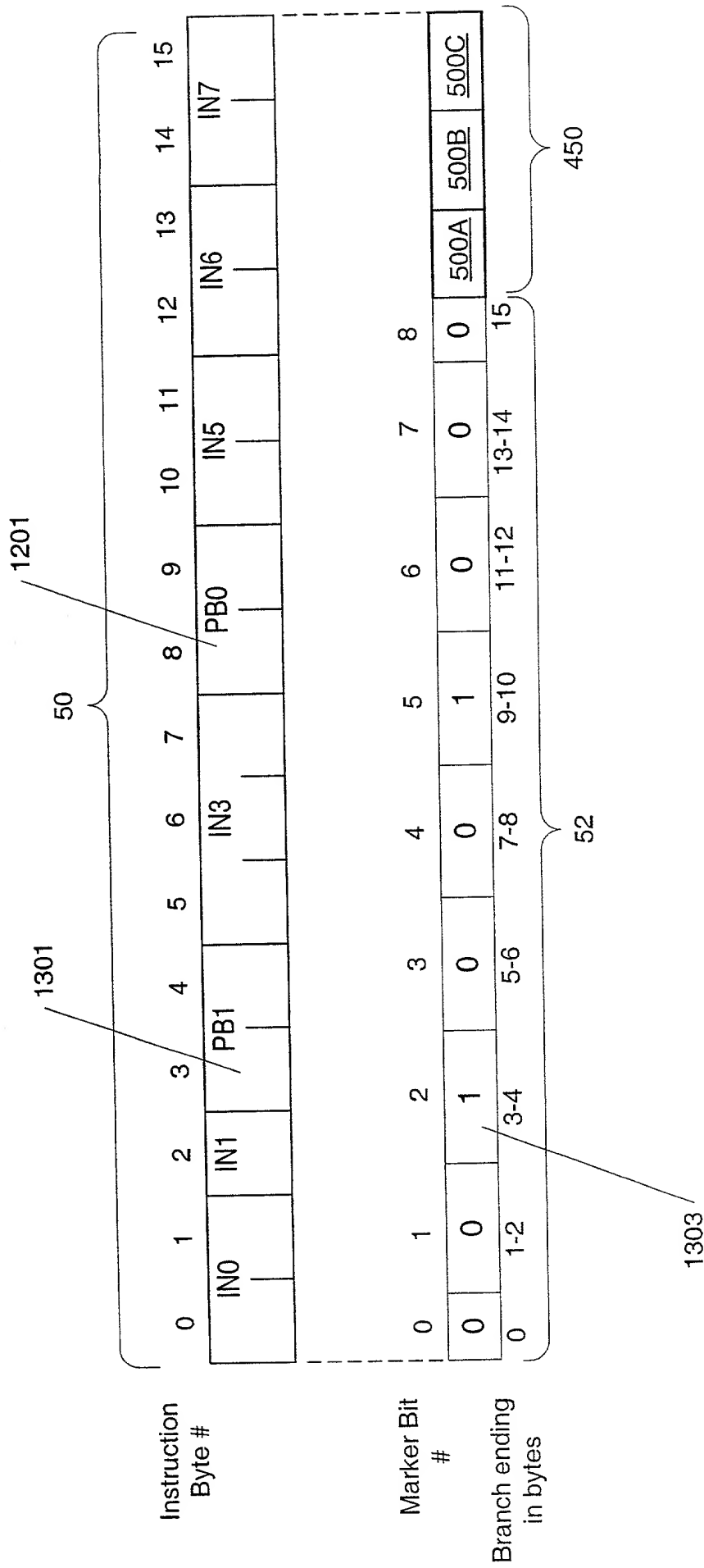


Fig. 12

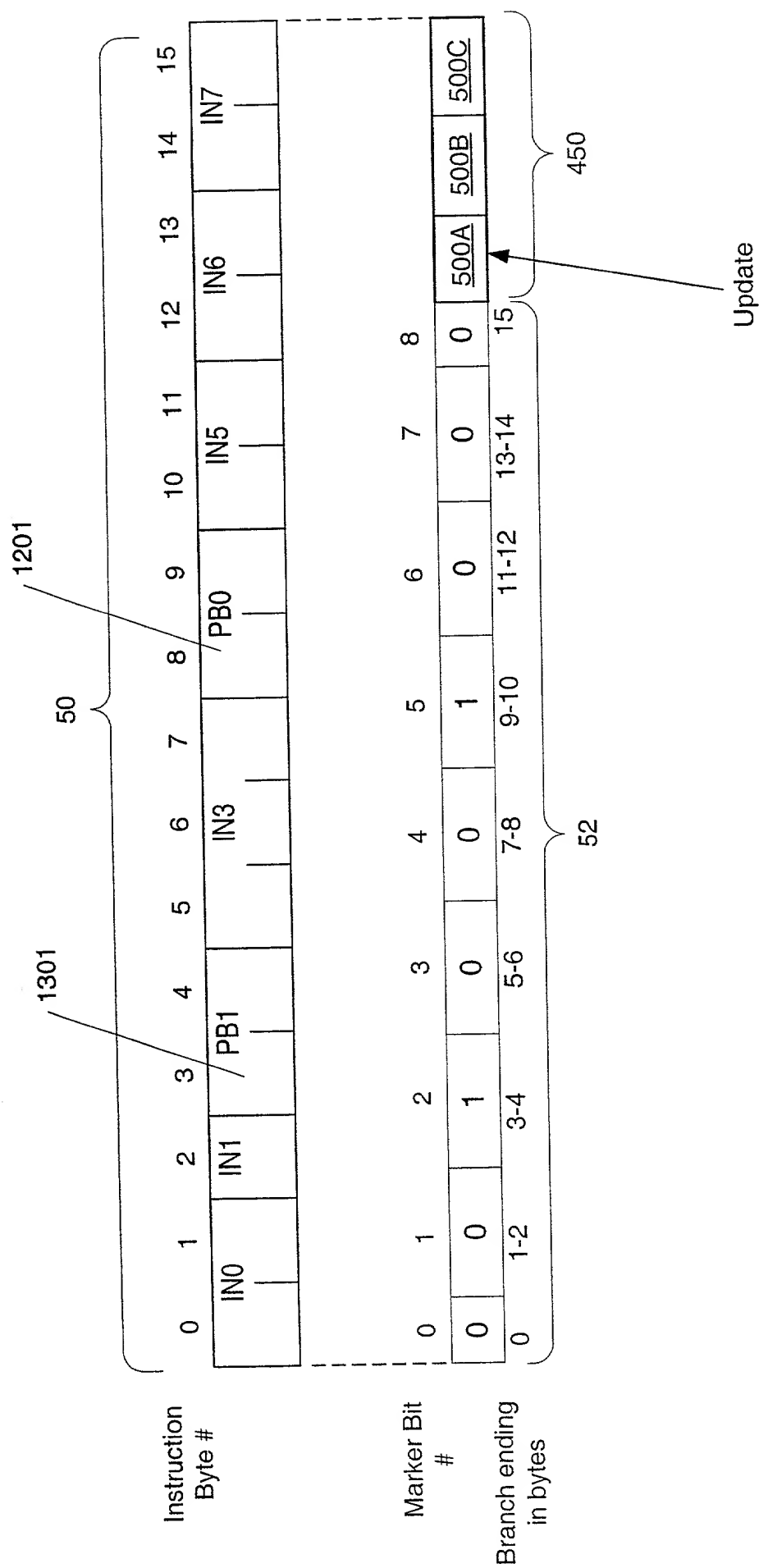


Fig. 13

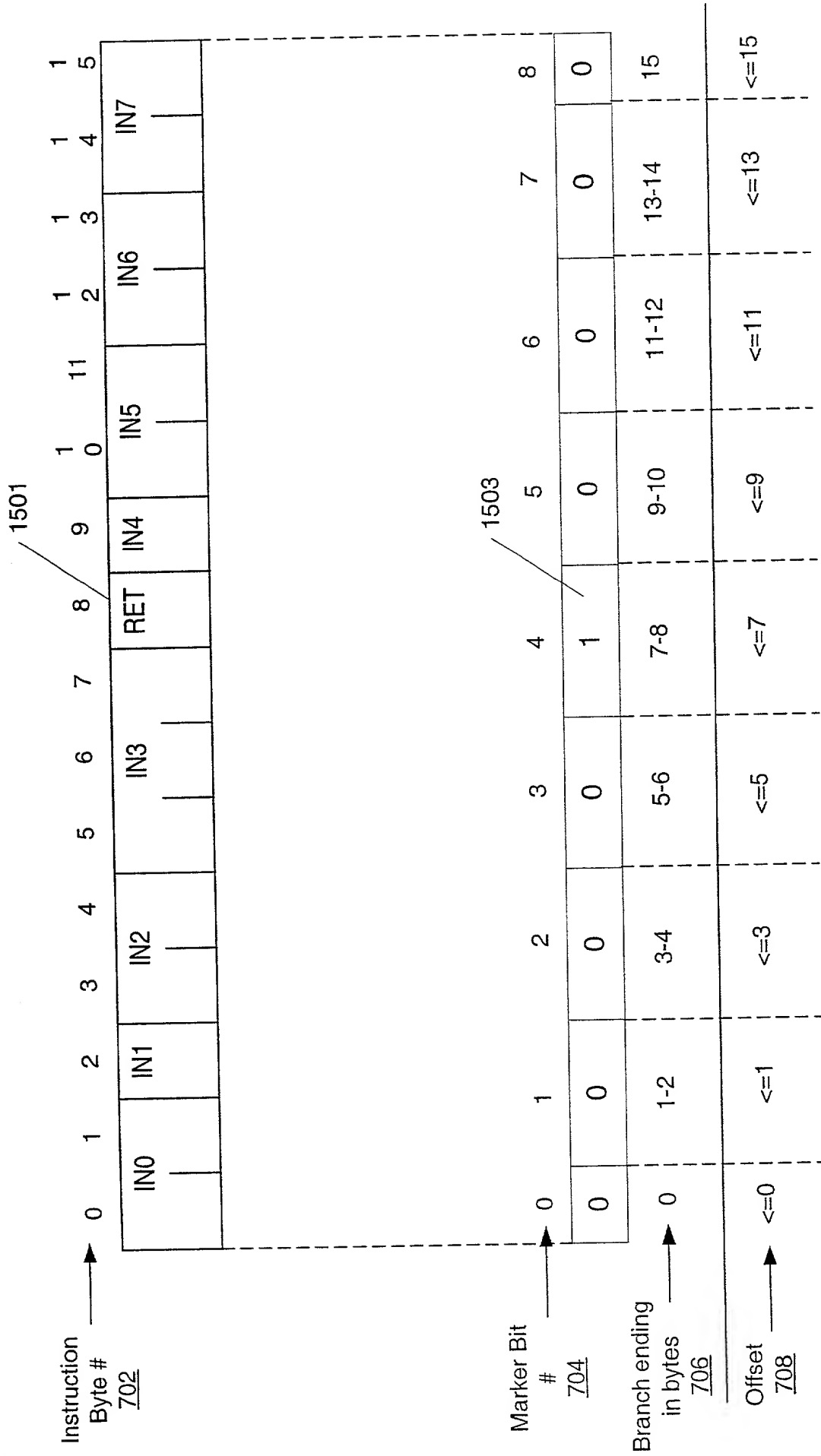


Fig. 14

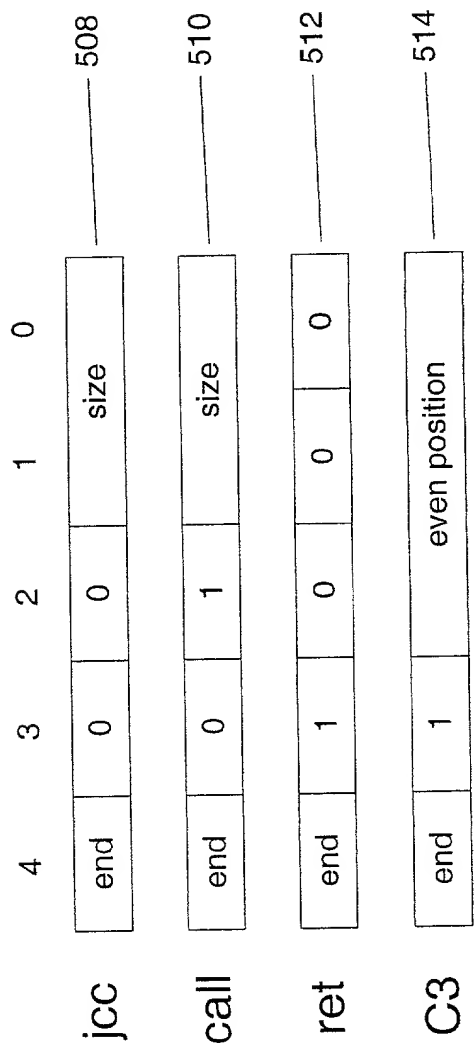
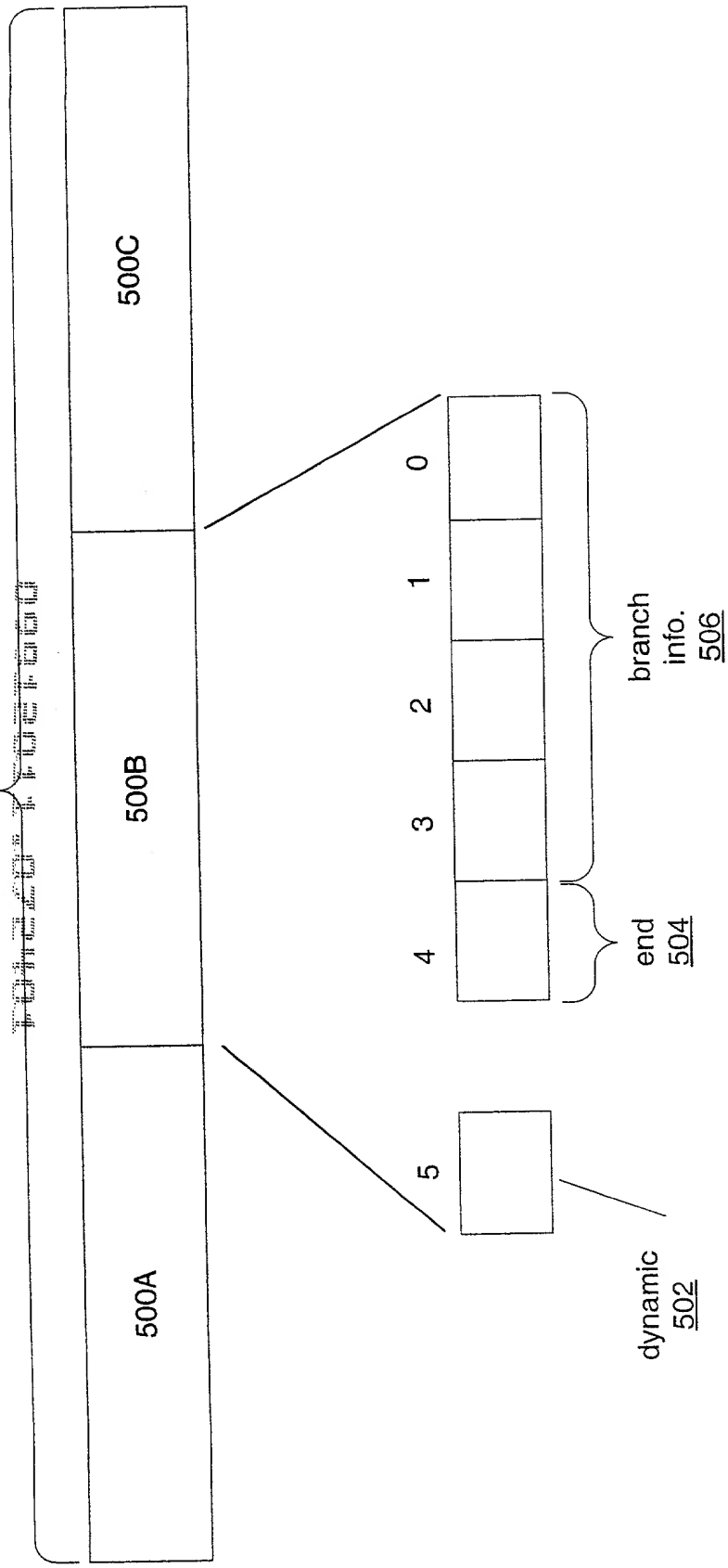


Fig. 15

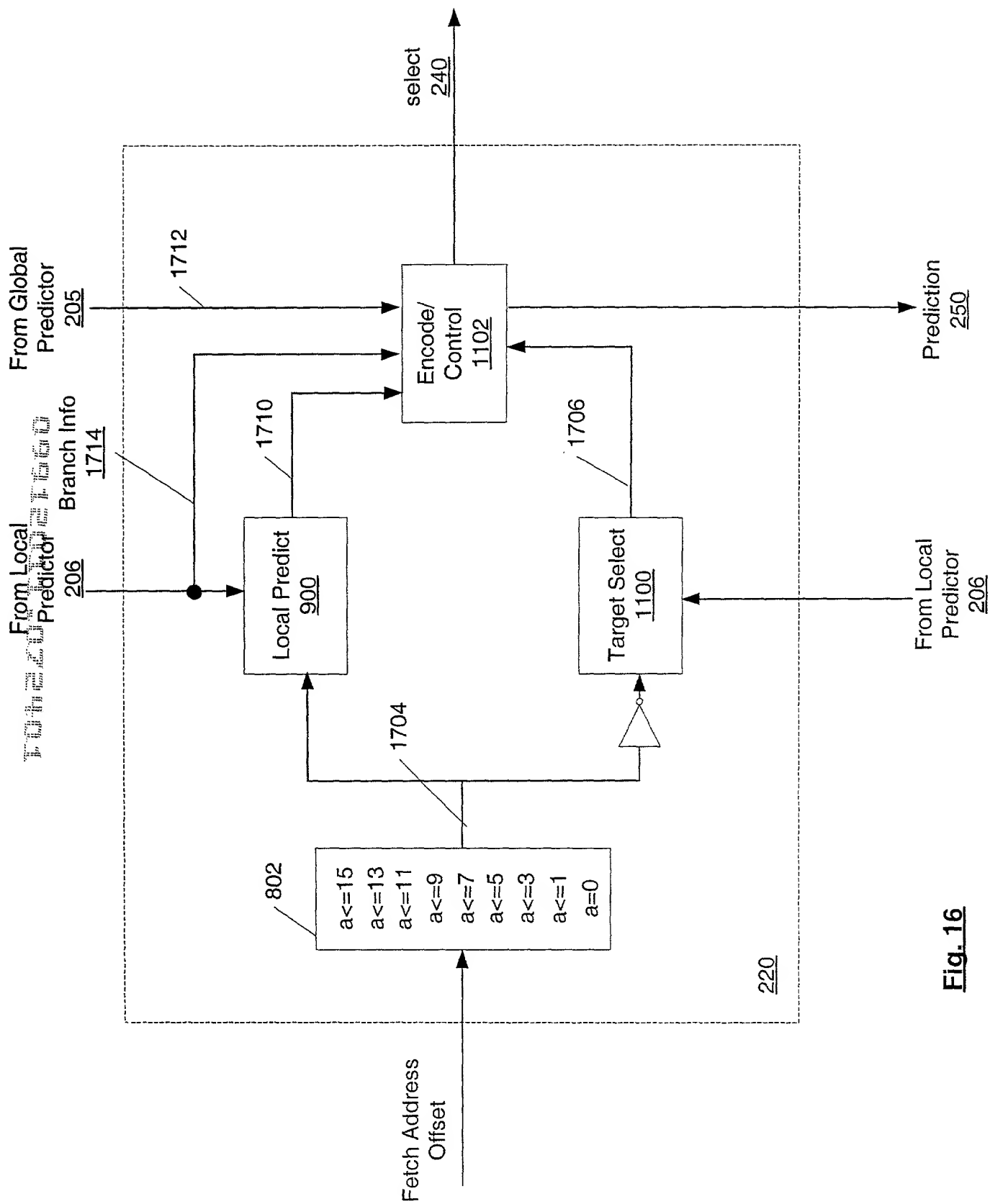


Fig. 16

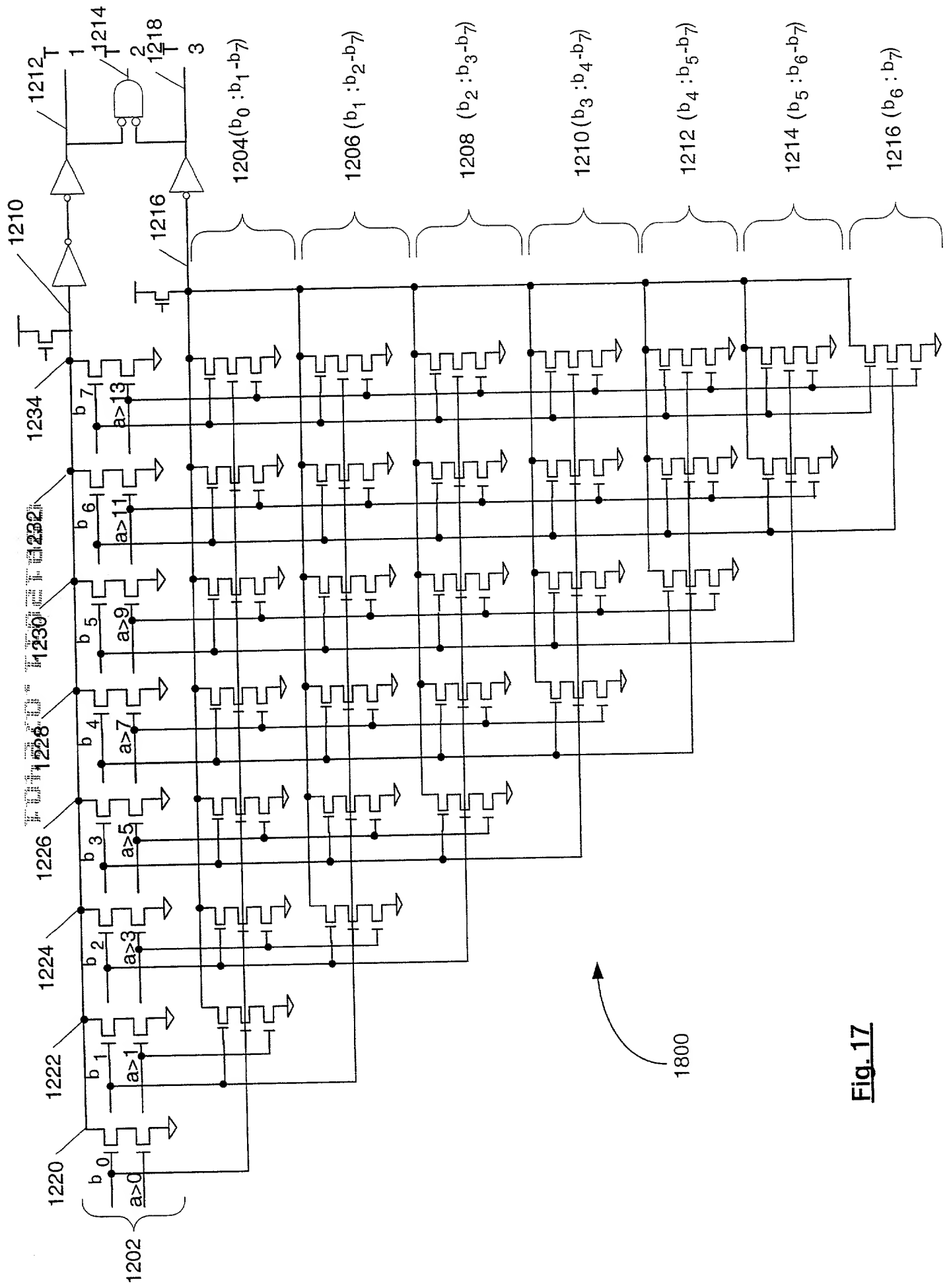


Fig. 17

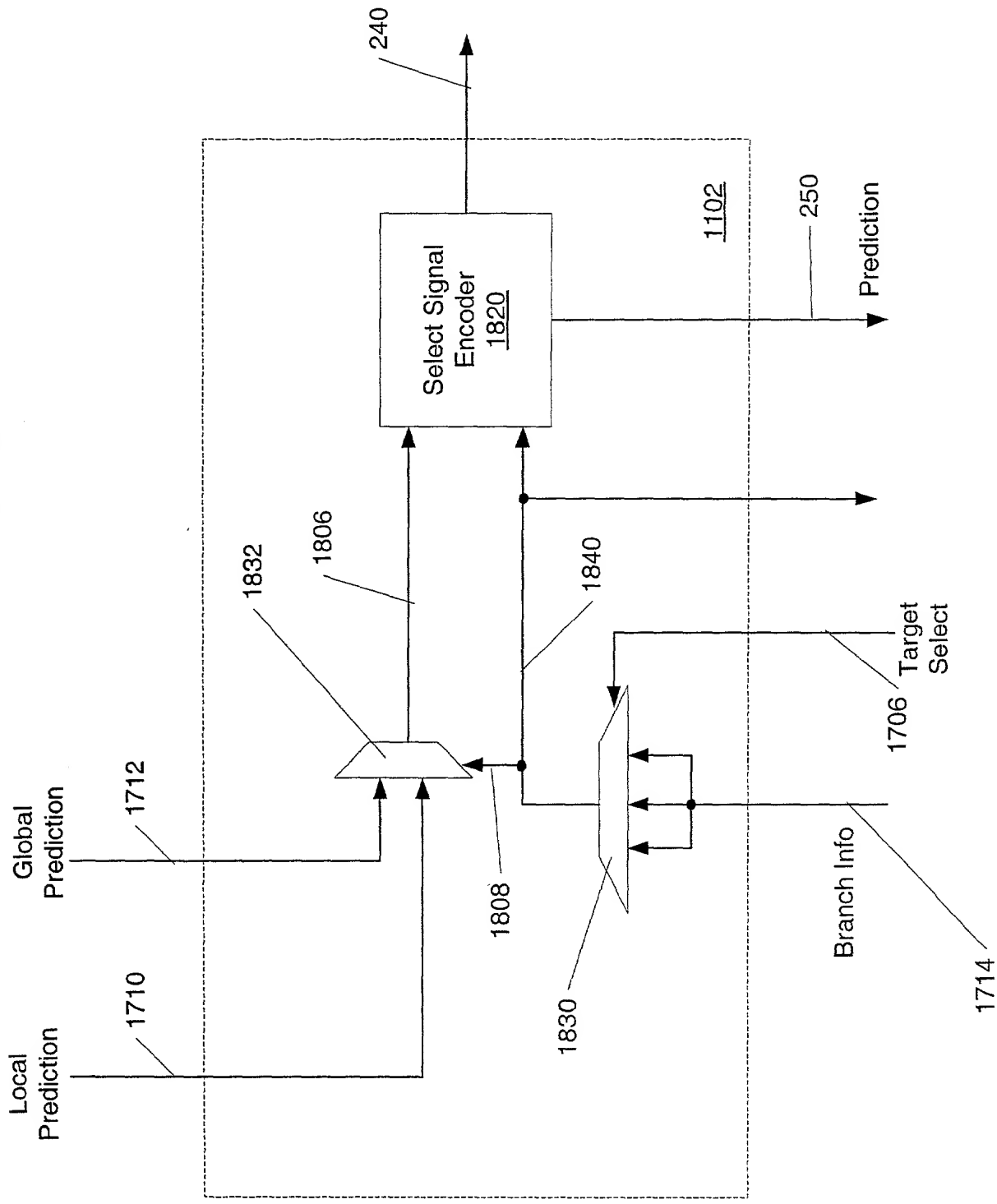


Fig. 18

From Prediction
Logic 220
From Cache 160

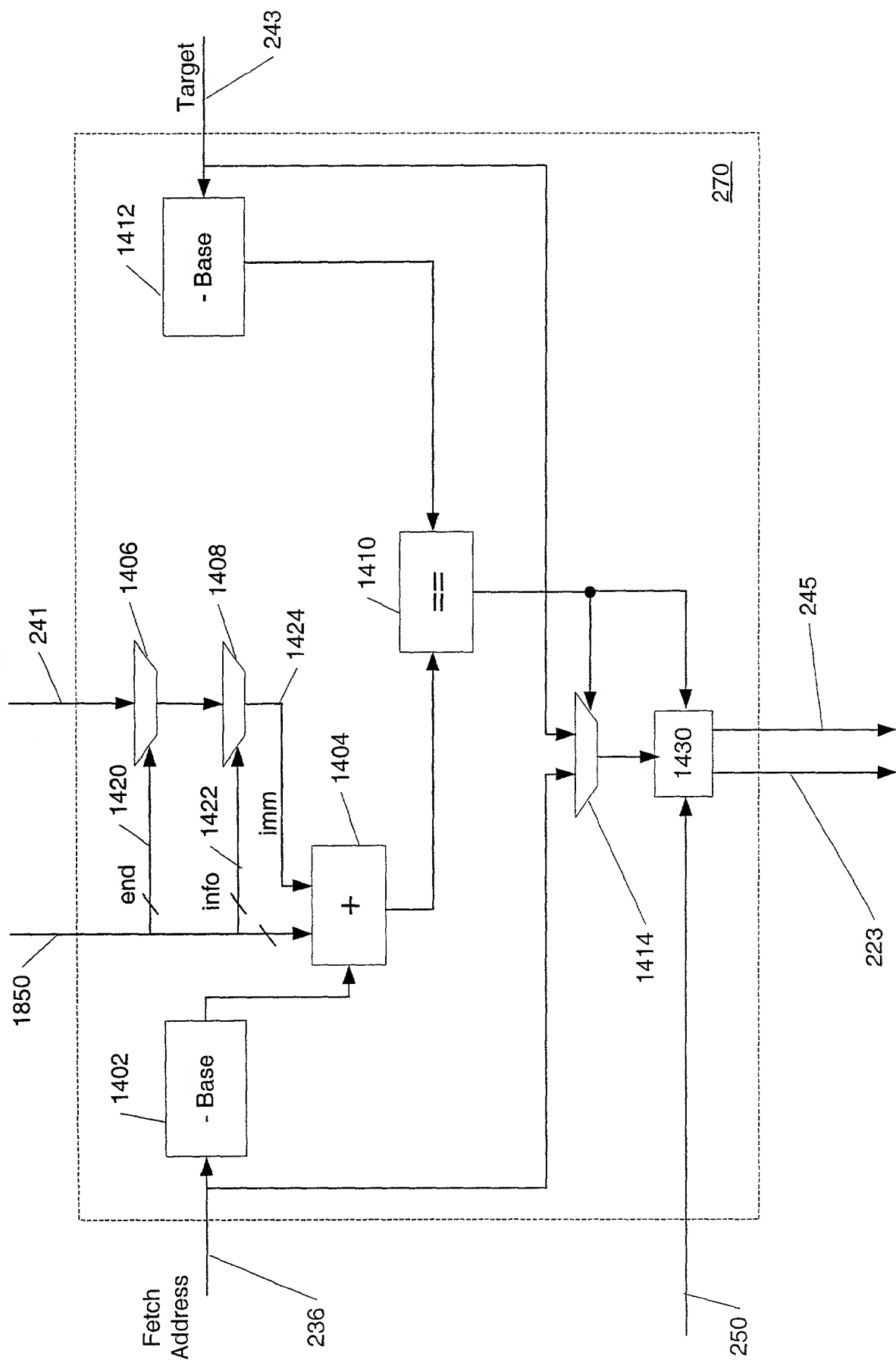


Fig. 19

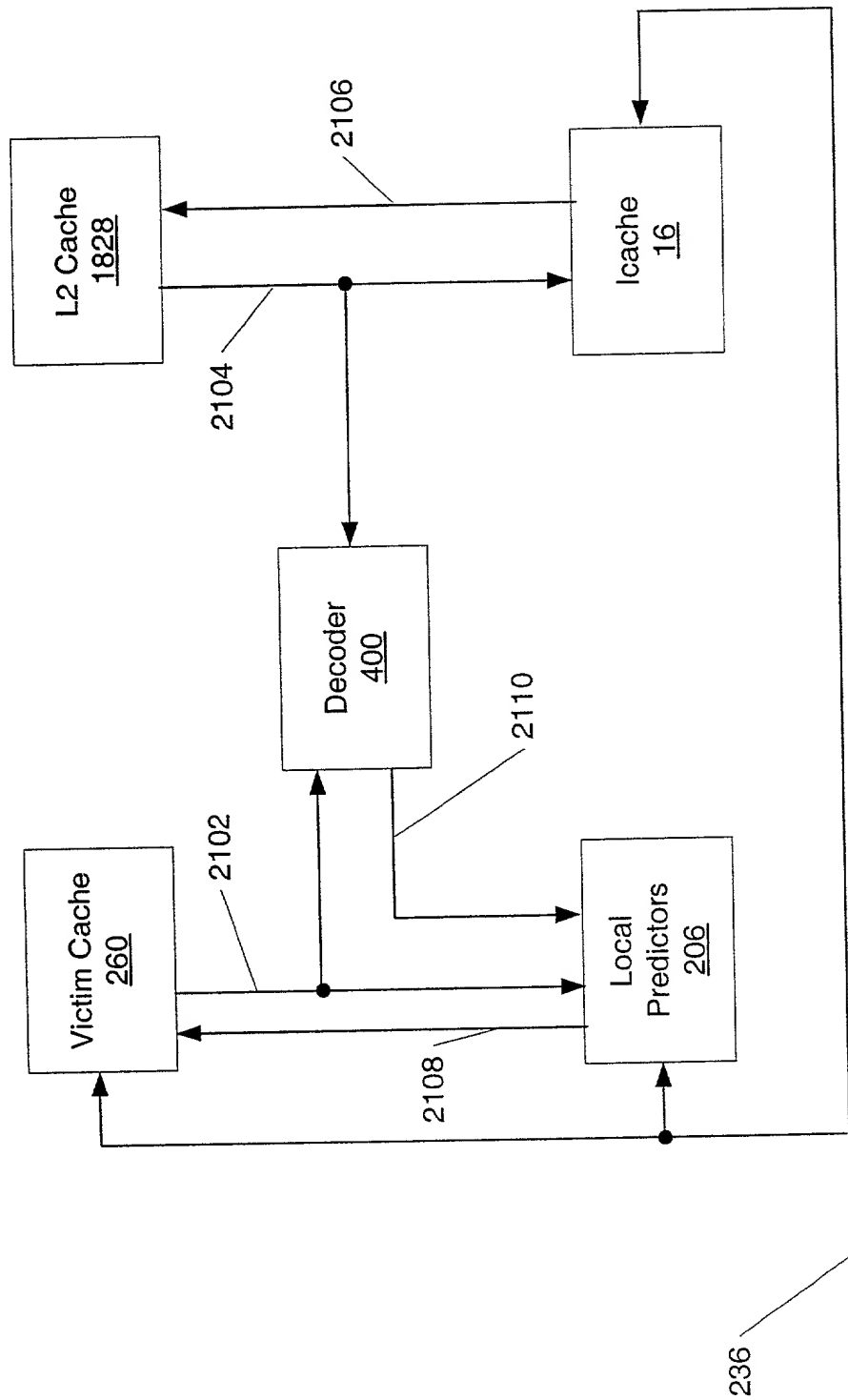


Fig. 20

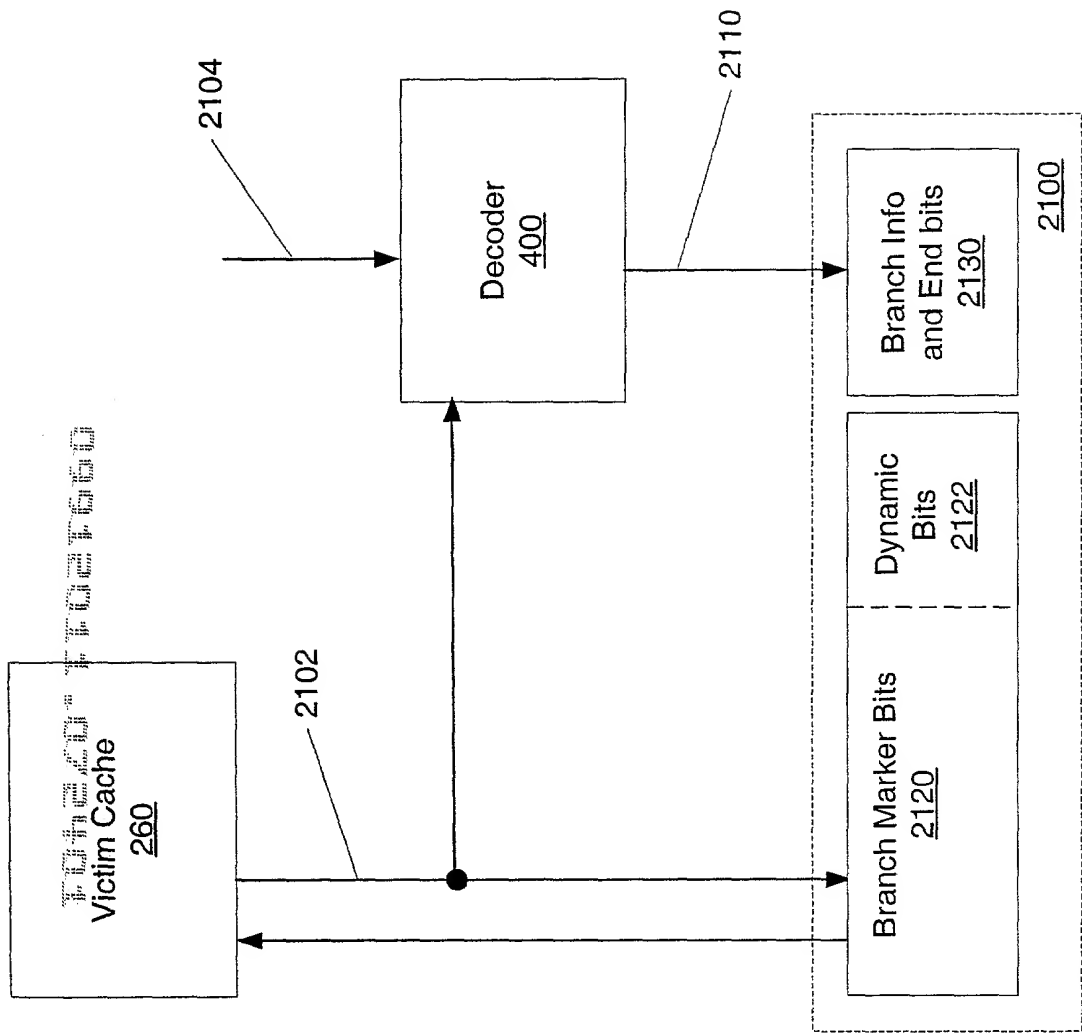


Fig. 21

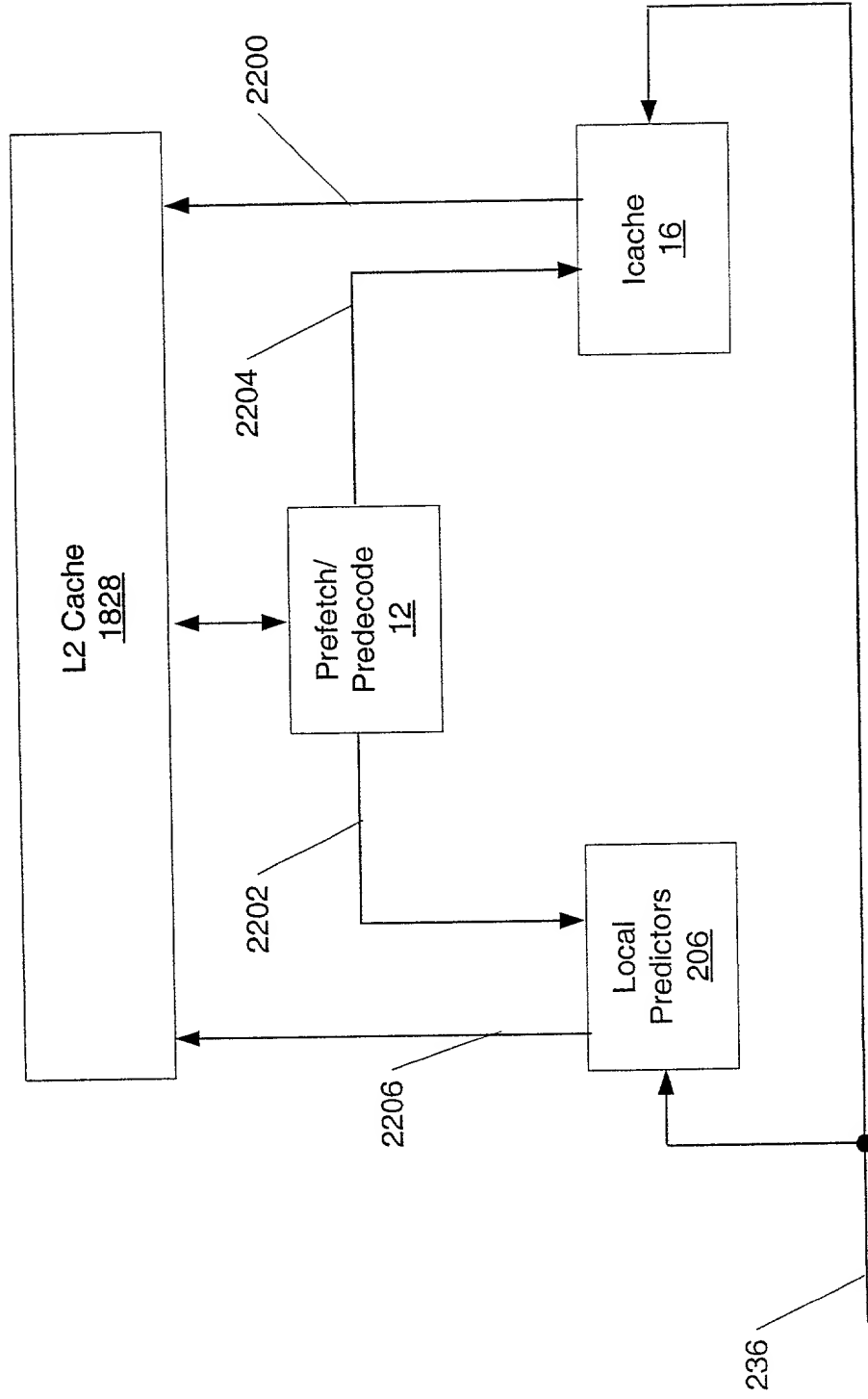


Fig. 22

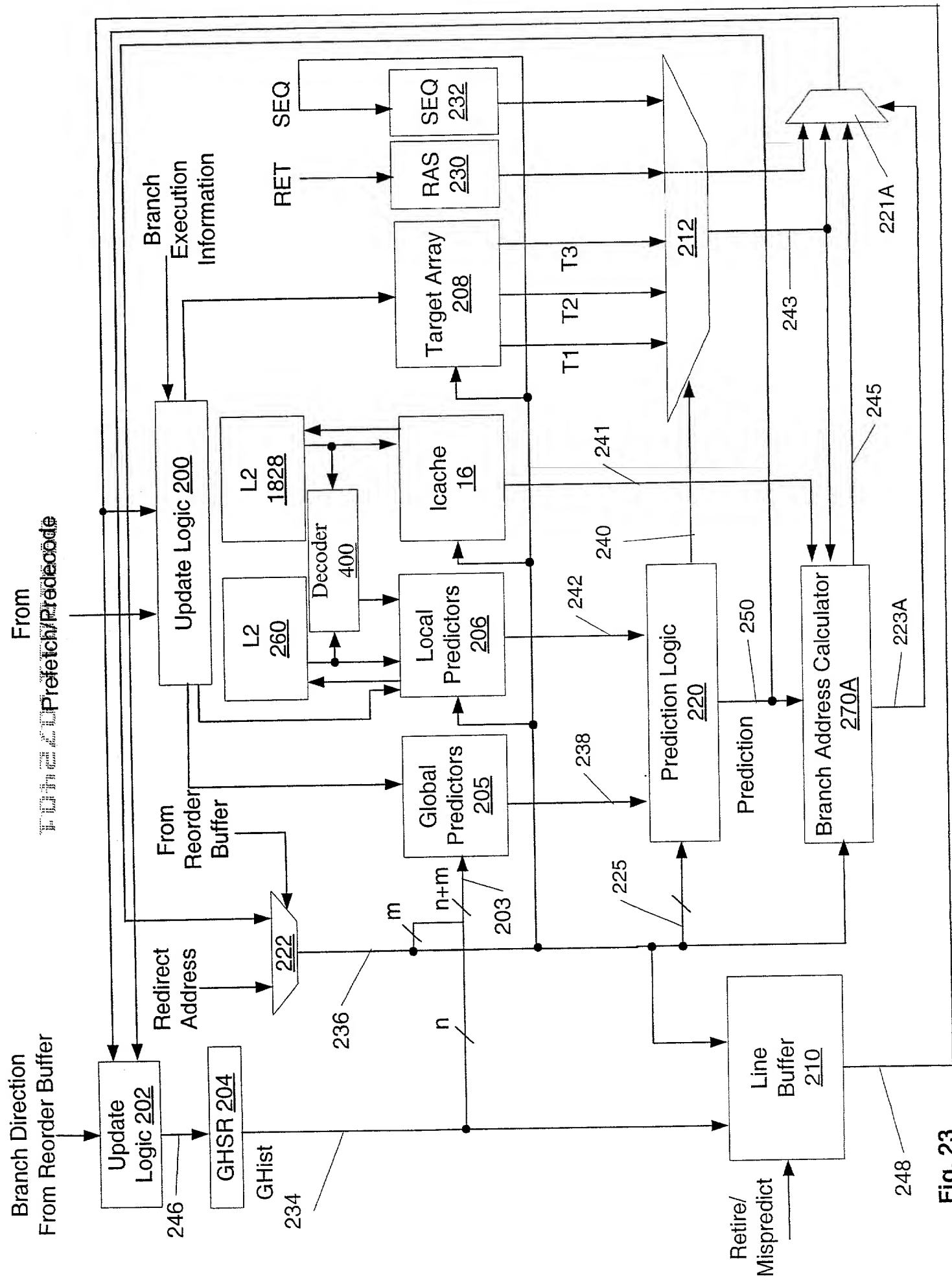


Fig. 23



Fig. 24

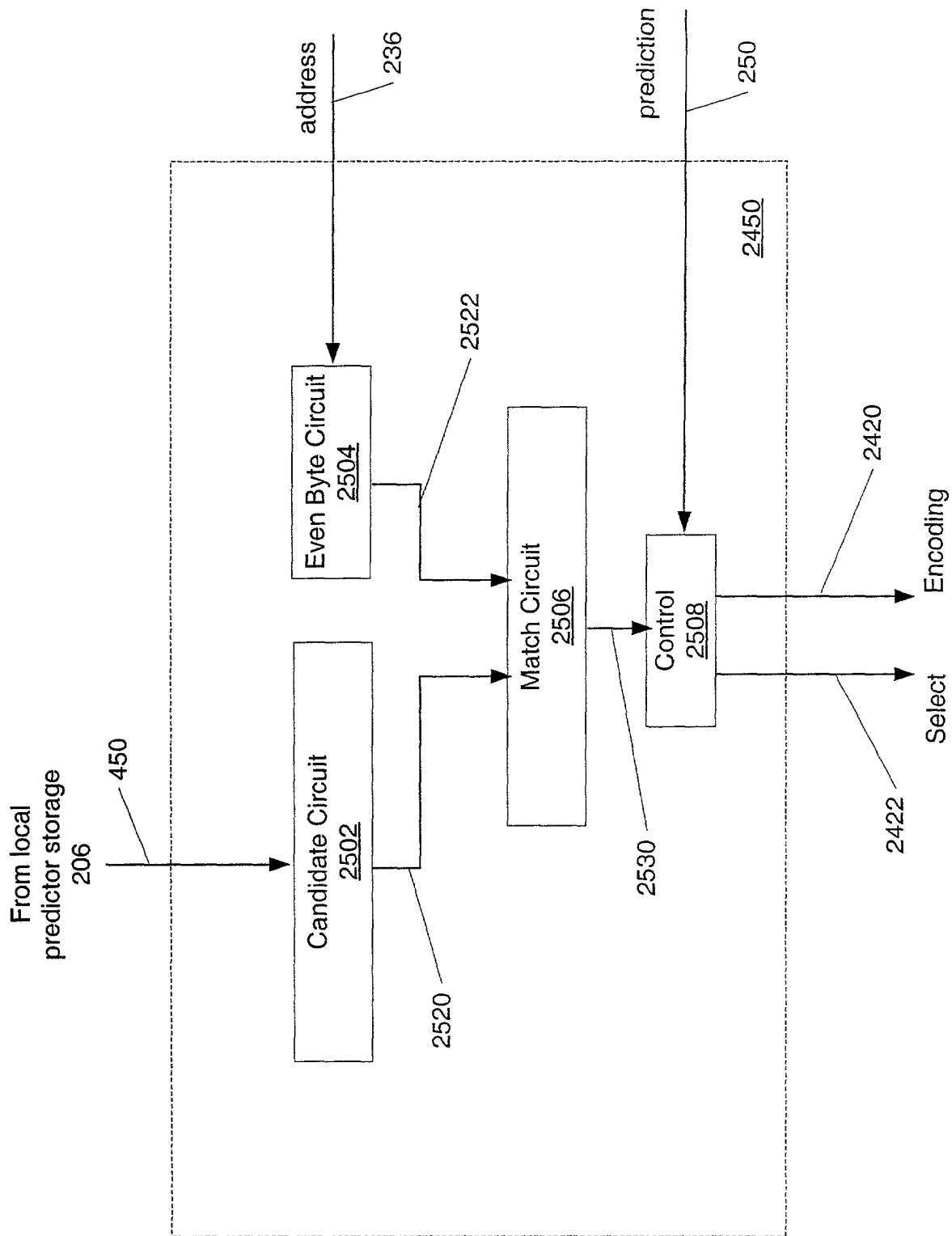


Fig. 25

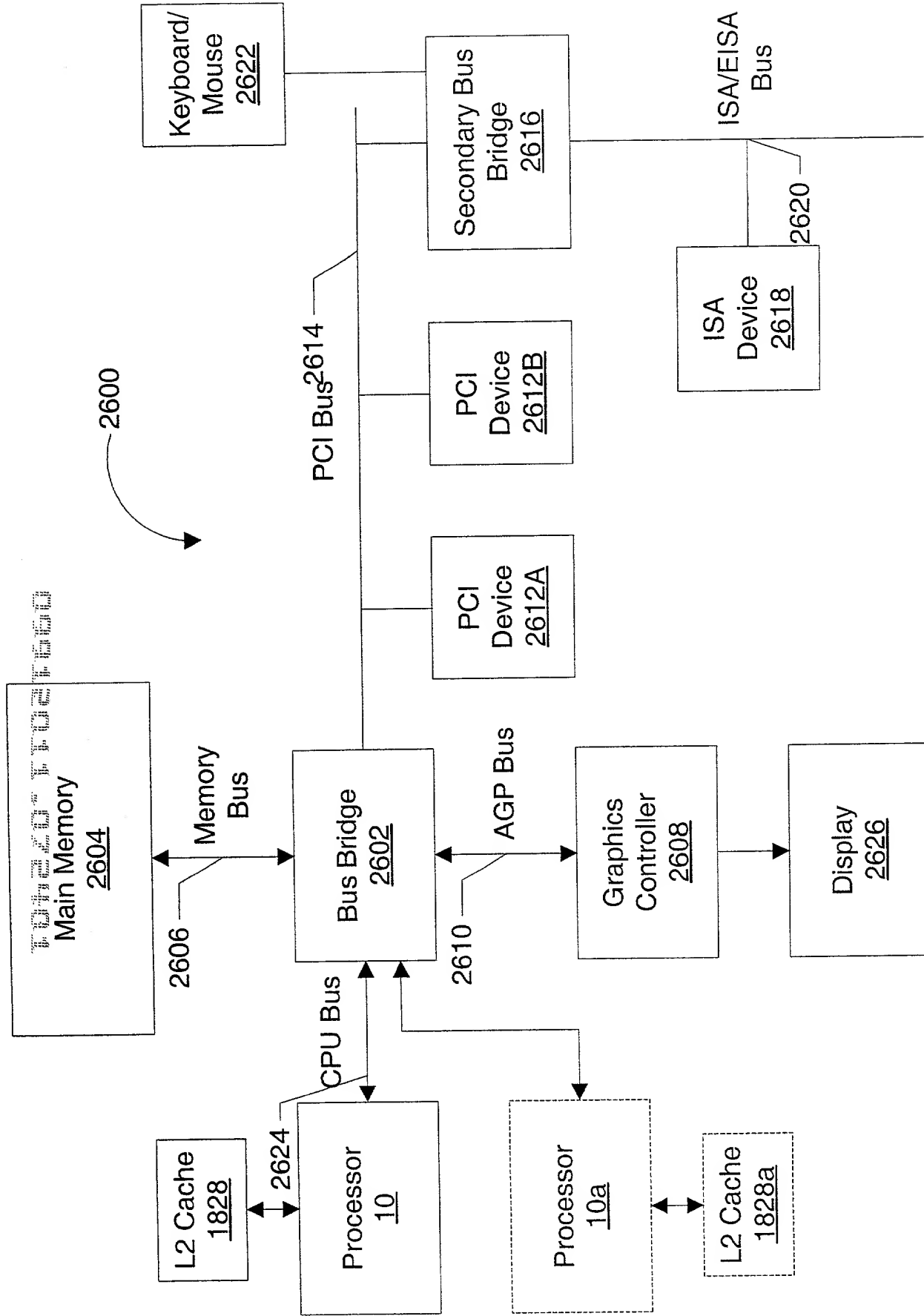


Fig. 26